EXHIBIT 1

REDACTED IN ITS ENTIRETY

EXHIBIT 2

REDACTED IN ITS ENTIRETY

EXHIBIT 3

UNITED STATES DISTRICT COURT

DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC.,	)Civil Action No.
Plaintiff/Counterclaim	)04-875-GMS
Defendant,	)
vs.	)
LUCENT TECHNOLOGIES, INC.,	)
Defendant/Counterclaim	)
Plaintiff.	)
	)
TELCORDIA TECHNOLOGIES, INC.,	)Civil Action No.
Plaintiff/Counterclaim	)04-876-GMS
Defendant,	)
vs.	)
CISCO SYSTEMS, INC.,	)
Defendant/Counterclaim	)
Plaintiff.	) VOLUME II
	) PAGES 270 - 493

CERTIFIED COPY

CONFIDENTIAL - PURSUANT TO PROTECTIVE ORDER

VIDEOTAPED DEPOSITION OF

ANTHONY ACAMPORA, PH.D., taken at 333 West Harbor Drive, San Diego, California, at 9:41 a.m., Thursday, August 3, 2006, before Elaine Smith, CSR No. 5421

are limits, correct?

A. Can you show me what you're pointing to?

Q. Would you look on the Bates page 609.

A. Any particular --

Q. Just above Table 1.

A. The paragraph titled "Access Control"?

Q. Yes.

A. Okay.

Q. The paragraph under that, five lines down, it says, "When it --" referring to each station, "When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again."

A. It says that. But if we look on the very next page, the top line, it also says, "If a station has priority, it is given permission to access the line for an integral number of slots." It would make no sense to access for a non-integral number. So you give permission to access for an integral number of slots without specifying just how large that integer number might be. So it could be any

number. Essentially, it could be so big as to mean if I have something to send, I will seize each and every slot.

Q. In other words, you're saying that a system that has access limits could always be adjusted to remove the access limits, in which case it would be like the '306 Patent, correct?

MS. MEHTA: Objection as to form. Foundation. And incomplete hypothetical.

THE WITNESS: And that's not what I said. What I said is, reading the Fasnet reference, one would understand that the authors recognize that although they stated in one place that, as an example, you can access only a single slot per cycle, they also recognize that you can access for more than a single slot per cycle. In fact, they don't specify how large that number may be. So one would recognize that they're showing that the one-slot-per-cycle access is not a fundamental limitation of what they're describing here. In fact, there is no limitation to what they're describing here.

EXHIBIT 4

REDACTED IN ITS ENTIRETY

EXHIBIT 5

NOS - DI # 118

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC., Plaintiff/Counterclaim Defendant, v. LUCENT TECHNOLOGIES INC., Defendant/Counterclaim Plaintiff.	)	Civil Action No. 04-875-GMS

LUCENT TECHNOLOGIES INC.'S OBJECTIONS AND SECOND SUPPLEMENTAL RESPONSE TO TELCORDIA TECHNOLOGIES, INC.'S INTERROGATORY NOS. 6 AND 7

Pursuant to FEDERAL RULES OF CIVIL PROCEDURE 26(d) and 33, Defendant/Counterclaim Plaintiff Lucent Technologies Inc. ("Lucent") by its attorneys, hereby objects and responds to Interrogatory Nos. 6 and 7 of Plaintiff/Counterclaim Defendant Telcordia Technologies, Inc.'s ("Telcordia") First Set of Interrogatories (the "Interrogatories") as follows:

GENERAL OBJECTIONS

Lucent incorporates by reference its General Objections in Lucent's Objections and Supplemental Responses to Telcordia Technologies, Inc.'s First Set of Interrogatories.

INTERROGATORIES

INTERROGATORY NO. 6

For each prior art reference that Lucent contends, whether taken separately or in combination, invalidates any claim of the Patent-In-Suit under 35 U.S.C. §§ 102 or 103, identify: (a) each claim in the Patent-In-Suit that Lucent contends is invalidated by the reference(s); (b) each fact known by Lucent that supports or refutes its contentions that each and every claim element or limitation is disclosed or suggested by specific teachings in the prior art reference; (c) all current or former officers, employees, agents, and consultants retained by or for Lucent who are most knowledgeable about each identified item of prior art and its relationship to the Patent-In-Suit; and (d) all documents relating to such prior art or Lucent's contentions.

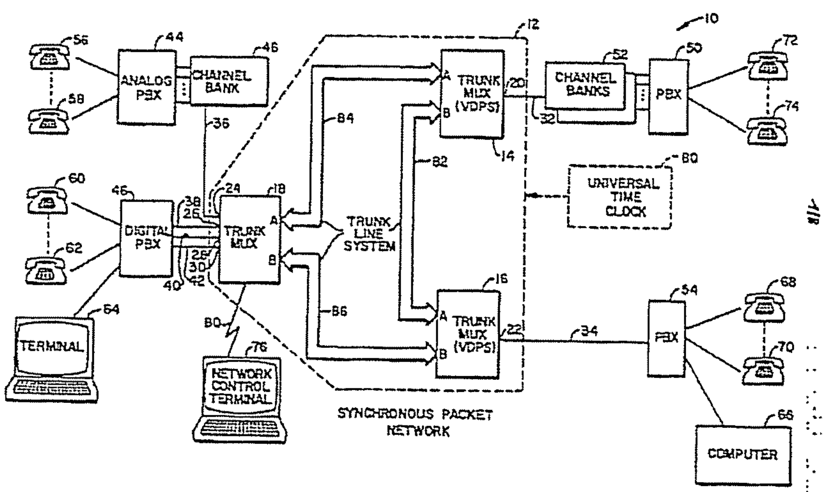
SECOND SUPPLEMENTAL RESPONSE

Lucent repeats and realleges all previous General Objections to Telcordia's Interrogatories and the Specific Objections to Interrogatory No. 6.

Lucent incorporates by reference Cisco's responses to Telcordia's Interrogatory No. 5 in *Telcordia Technologies, Inc. v. Cisco Systems, Inc.*, Civil Action No. 04-876 (GMS) (D. Del.).

Subject to and without waiving the foregoing objections, Lucent states that at least the following prior art references, individually and/or taken together, render the asserted claims of the '306 patent invalid under 35 U.S.C. §§ 102 and/or 103. In the following claim charts, Lucent uses the same application of the claims to the prior art references as Telcordia uses in its analysis of the allegedly infringing products, *see Telcordia Supplemental Responses to Lucent Interrogatory No. 1*:

Claim of U.S. Patent No. 4,893,306	**Disclosure in U.S. Patent No. 4,569,041 ("Takeuchi"), Issued Feb. 4, 1986**
1. A method for simultaneously transmitting data	Takeuchi discloses a method for simultaneously transmitting data from sources having different bit rates in a telecommunication network.

bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream.	*See, e.g.*, 12:20-28 ("The standard trunk frame for DS-1 as described in the Bell System Compatibility Bulletin Number 119 is 193 PCM bits at a data rate of 1.544 bps, corresponding to a clock rate of 1.544 MHz. In accordance with the invention, the entire frame forms a packet. The first bit is the standard DS-1 Framing Bit, the next 24 bits are set aside for packet overhead functions, and 168 bits are employed to convey voice or data.") *See, e.g.*, Fig. 1:  FIG._1.

U.S. Patent No. 4,893,306	**Description in Limb & Flores, "Description of Fasnet – A Unidirectional Local-Area Communications Network," The Bell System Technical Journal, Vol. 61, No. 7, September 1982 ("Fasnet")**
1. A method for simultaneously transmitting data from sources having different bit rates in a telecommunication network comprising the steps of:	Fasnet discloses a method for simultaneously transmitting data from sources having different bit rates in a telecommunication network. *See, e.g.*, p. 1415 ("An integrated transmission system simplifies the implementation of services that utilize different types of traffic. Examples are voice annotated electronic mail and interactive use of voice and facsimile.")
generating a bit stream comprising a sequence of frames,	Fasnet discloses generating a bit stream comprising a sequence of frames. *See, e.g.*, p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has

	been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.") *See, e.g.*, p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B. The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.")
each of said frames including a transmission overhead field containing frame timing information and an empty payload field, and	Fasnet discloses that each of the frames includes a transmission overhead field containing frame timing information and an empty payload field. *See, e.g.*, p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium. The main objective in the design of this field is to control access among all active stations in an efficient, reliable, and fair manner. The frame start and frame end delimiters are unnecessary, since the stations are kept in tight bit and frame synchronization (see Section 5.1). The duration of the frame is referred to as a slot.") *See, e.g.*, Table 1:

Table I—Protocol and frame structures

	Protocol Structure	Frame Structure
Data link layer	Logical link control sublayer	DA/SA/LC/IU
	Media access control sublayer	FS/AC/DA/SA/LC/IU/FCS/FE
Physical layer	Physical layer signaling	FS/AC/DA/SA/LC/IU/FCS/FE

FS: Frame starting delimiter
AC: Access control field
DA: Destination address
SA: Source address
LC: Link control field
IU: Information unit from network layer
FCS: Frame check sequence
FE: Frame ending delimiter

See, e.g., Fig. 3:

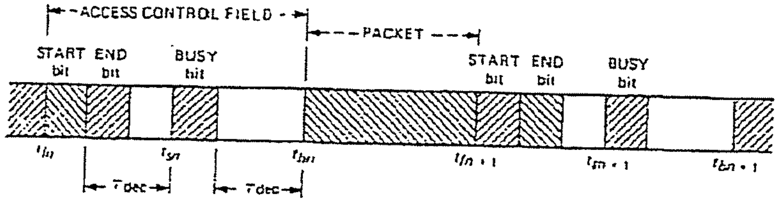


Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer.

See, e.g., p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.");

See, e.g., p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B. The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.")

See, e.g., pp. 1425-26 ("V. IMPLEMENTATION

	CONSIDERATIONS The design criteria previously stressed in the introduction affect the implementation in important ways. In particular, the requirement to operate at high speeds and the unidirectional operation of the bus affect the design of the synchronization system; in turn, the type of synchronization and the use of directional couplers impact the choice of the line code that is used. 5.1 Synchronization Bus systems in which signals travel in both directions on the line require the receiving stations to adapt to the signals transmitted by the sending station because the amplitude, dispersion, and phasing of the received signal vary depending upon the position of the transmitting station on the line. Synchronization can be achieved very quickly when the signaling rate is low relative to the bandwidth of the transmission medium. At higher signaling rates, synchronization needs to be more accurate to achieve good error performance. Ethernet specifies a synchronization preamble of 64 bits and for higher transmission rates an even longer sequence may be required. Thus, for short messages efficiency would be significantly reduced. Using a unidirectional bus, each station can be synchronized to a common clock issued from the head station. Thus, if all stations add signals to the cable in phase with the transmitting clock, stations will receive the signals in correct phase. Similarly, fixed gain and frequency compensation can be employed. The problem of reliability can be overcome by giving each station the ability to supply clock. The clock drive would be inhibited by detection of, and locking to, an incoming clock. Initial tests have shown that a simple, cost-effective method of synchronization is to synchronize to a continuously injected pilot tone placed at the high end of the signaling band. The synchronizing function then assumes a negligible fraction of the transmission capacity. In addition to bit synchronization, frame synchronization is also required. This is achieved by sending periodically a synchronizing bit pattern. Design is simplified if this is sent after an integral number of frames, say 64 or 128. With tight bit and frame synchronization, successive frames may be butted together without a gap.")
filling the empty payload fields in said frames with	Fasnet discloses filling the empty payload fields with data in packetized format from a plurality of sources which have access to the bit stream, including circuit or packet sources.

data in packetized format from a plurality of sources which have access to the bit stream including circuit or packet sources,

See, e.g., p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium.")

See, e.g., Table 1:

Table I—Protocol and frame structures

	Protocol Structure	Frame Structure
Data link layer	Logical link control sublayer Media access control sublayer	DA/SA/LC/IU FS/AC/DA/SA/LC/IU/FCS/FE
Physical layer	Physical layer signaling	FS/AC/DA/SA/LC/IU/FCS/FE

FS: Frame starting delimiter
AC: Access control field
DA: Destination address
SA: Source address
LC: Link control field
IU: Information unit from network layer
FCS: Frame check sequence
FE: Frame ending delimiter

See, e.g., Fig. 3:

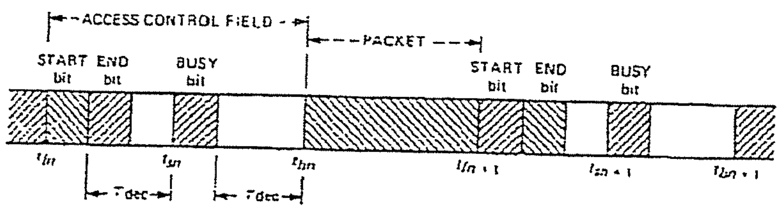


Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer.

See, e.g., p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.")

See, e.g., 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized

	depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.")
such that data in packetized format from any of said sources is written into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously via said bit stream.	Fasnet discloses that data in packetized format from any of the sources is written into any available empty payload of the frames for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from the plurality of sources simultaneously via the bit stream. *See, e.g.*, p. 1419 ("If a station has priority, it is given permission to access the line for an integral number of slots. In this manner, the active stations can access the line for a specified duration in the order in which they are physically located on the line.") *See, e.g.*, p. 1427 ("VI. IMPROVING UTILIZATION As can be seen from (I), efficiency increases (i) as cycle length increases and (ii) as the idle period at the end of each cycle (intercycle gap) decreases. At the expense of some increase in complexity, techniques may be devised to improve utilization by increasing cycle length or reducing intercycle gap. 6.1 Control of cycle length Since START = 1 may be read by all stations, the length of the last cycle, τc, may be determined by any station. As previously described, each station may transmit up to p_{max} packets per access. Thus, by controlling p_{max}, stations may influence the value of τ_c. Station control of τ_c by manipulation of p_{max} is obviously limited. For example, let us assume that p is fixed at 1 and that we have stations each generating packets at a rate $<1/\tau_c$. Increasing p will not change the cycle length since packets will be transmitted before a queue can form. On the other hand, increasing p for heavily loaded stations will lead to an increase of τ_c provided τ_c is less than the accepted maximum.") *See, e.g.*, p. 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.") *See, e.g.*, p. 1432 ("ACCESS-A station has a connection. Stations that already have access take the first free slot available to them after the appropriate START. Allocation of freed up slots on

	a reasonably equitable basis would proceed as follows. Stations would be aware of say n slots becoming free from the position of the END bit on the return line. Note, no END is issued if the class is full. Stations in the DEFER state would be permitted to compete for the n empty slots at the end of the subcycle. This will favor stations close to the head end. However, a large degree of fairness is achieved by permitting stations to switch from the WAIT to DEFER state only when two consecutive ENDS are encountered for that subcycle. This will only occur when all traffic currently in DEFER state has been granted access. At this point, traffic in the WAIT state would switch to DEFER and then vie for empty slots as they become available. This strategy is related to the snapshot algorithm. (iv) Continuation-In contrast to blocking, continuation requires that traffic not able to access the link in the previous cycle be served before any new traffic is accommodated. This may be achieved in the following manner. Assume that the class type is non-blocking. If the head station should issue a new START before all traffic of the class has been served, the end station will not detect the end of the cycle and hence will not issue END = 1. The absence of an END = 1 would indicate to the head station that the p registers of the stations in that class should not be reset on the next cycle (i.e., the stations would not switch from WAIT to DEFER). Thus, in the following cycle, remaining traffic would be served. For centralized control, the START for this traffic type could contain an additional bit to indicate whether the previous cycle is being continued for deferring tragic or a fresh cycle is being started for new traffic. For distributed control, each station could keep track of the sequence of STARTS and ENDS. It is important that the control strategy be adaptive to changing traffic conditions. We expect that the traffic mix will change relatively slowly-over a period of seconds rather than ms. Thus, it would be feasible to have the adaptation achieved by a server process. The control algorithm could be implemented as completely distributed, completely centralized, or somewhere in between. Economics and reliability will dictate, to a large extent, where the control should be placed. Nevertheless, a hybrid strategy would seem more in the spirit of the current design. For example, selection is probably best achieved by having the head station transmit the appropriate START code (centralized, but perhaps assumable), whereas traffic assignment and continuation is probably best achieved by having each station read and operate on

	the END field (distributed).")
3. A method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources comprising	Fasnet discloses a method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources. *See, e.g.*, p. 1415 ("An integrated transmission system simplifies the implementation of services that utilize different types of traffic. Examples are voice annotated electronic mail and interactive use of voice and facsimile.")
generating a bit stream comprising a sequence of frames,	Fasnet discloses generating a bit stream comprising a sequence of frames. *See, e.g.*, p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.") *See, e.g.*, p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B. The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.")
each of said frames including a transmission overhead field containing frame timing information and an empty payload field,	Fasnet discloses that each of the frames includes a transmission overhead field containing frame timing information and an empty payload field. *See, e.g.*, p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link

control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium. The main objective in the design of this field is to control access among all active stations in an efficient, reliable, and fair manner. The frame start and frame end delimiters are unnecessary, since the stations are kept in tight bit and frame synchronization (see Section 5.1). The duration of the frame is referred to as a slot.")

See, e.g., Table 1:

Table I—Protocol and frame structures

	Protocol Structure	Frame Structure
Data link layer	Logical link control sublayer	DA/SA/LC/IU
	Media access control sublayer	FS/AC/DA/SA/LC/IU/FCS/FE
Physical layer	Physical layer signaling	FS/AC/DA/SA/LC/IU/FCS/FE

FS: Frame starting delimiter
AC: Access control field
DA: Destination address
SA: Source address
LC: Link control field
IU: Information unit from network layer
FCS: Frame check sequence
FE: Frame ending delimiter

See, e.g., Fig. 3:

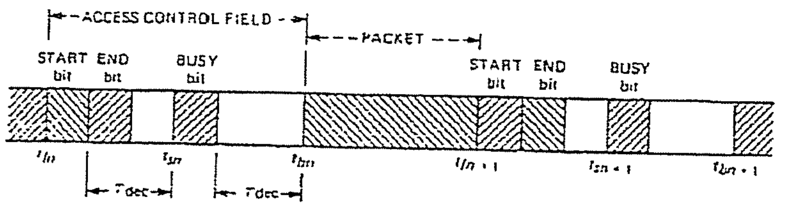


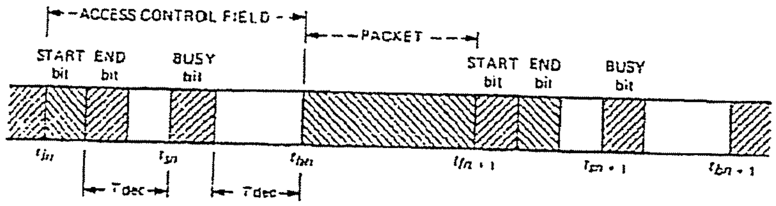
Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer.

See, e.g., p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.")

See, e.g., p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the

	frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B. The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.") *See, e.g.*, pp. 1425-26 ("V. IMPLEMENTATION CONSIDERATIONS The design criteria previously stressed in the introduction affect the implementation in important ways. In particular, the requirement to operate at high speeds and the unidirectional operation of the bus affect the design of the synchronization system; in turn, the type of synchronization and the use of directional couplers impact the choice of the line code that is used. 5.1 Synchronization Bus systems in which signals travel in both directions on the line require the receiving stations to adapt to the signals transmitted by the sending station because the amplitude, dispersion, and phasing of the received signal vary depending upon the position of the transmitting station on the line. Synchronization can be achieved very quickly when the signaling rate is low relative to the bandwidth of the transmission medium. At higher signaling rates, synchronization needs to be more accurate to achieve good error performance. Ethernet specifies a synchronization preamble of 64 bits and for higher transmission rates an even longer sequence may be required. Thus, for short messages efficiency would be significantly reduced. Using a unidirectional bus, each station can be synchronized to a common clock issued from the head station. Thus, if all stations add signals to the cable in phase with the transmitting clock, stations will receive the signals in correct phase. Similarly, fixed gain and frequency compensation can be employed. The problem of reliability can be overcome by giving each station the ability to supply clock. The clock drive would be inhibited by detection of, and locking to, an incoming clock. Initial tests have shown that a simple, cost-effective method of

	synchronization is to synchronize to a continuously injected pilot tone placed at the high end of the signaling band. The synchronizing function then assumes a negligible fraction of the transmission capacity. In addition to bit synchronization, frame synchronization is also required. This is achieved by sending periodically a synchronizing bit pattern. Design is simplified if this is sent after an integral number of frames, say 64 or 128. With tight bit and frame synchronization, successive frames may be butted together without a gap.")
packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets, and	Fasnet discloses packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets. *See, e.g.*, p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium.") *See, e.g.*, Table 1: Table I—Protocol and frame structures Protocol Structure / Frame Structure Data link layer: Logical link control sublayer — DA/SA/LC/IU; Media access control sublayer — FS/AC/DA/SA/LC/IU/FCS/FE Physical layer: Physical layer signaling — FS/AC/DA/SA/LC/IU/FCS/FE FS: Frame starting delimiter; AC: Access control field; DA: Destination address; SA: Source address; LC: Link control field; IU: Information unit from network layer; FCS: Frame check sequence; FE: Frame ending delimiter *See, e.g.*, Fig. 3:

	 Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer. *See, e.g.*, p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.") *See, e.g.*, 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.")
inserting said packets from said sources into the empty payload fields of said frames such that a packet from any of said sources is inserted into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously using said bit	Fasnet discloses that data in packetized format from any of the sources is inserted into any available empty payload of the frames for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from the plurality of sources simultaneously via the bit stream. *See, e.g.*, p. 1419 ("If a station has priority, it is given permission to access the line for an integral number of slots. In this manner, the active stations can access the line for a specified duration in the order in which they are physically located on the line.") *See, e.g.*, p. 1427 ("VI. IMPROVING UTILIZATION As can be seen from (I), efficiency increases (i) as cycle length increases and (ii) as the idle period at the end of each cycle (intercycle gap) decreases. At the expense of some increase in complexity, techniques may be devised to improve utilization by increasing cycle length or reducing intercycle gap. 6.1 Control of cycle length Since START = 1 may be read by all stations, the length of the last

stream.	cycle, τc, may be determined by any station. As previously described, each station may transmit up to p_{max} packets per access. Thus, by controlling p_{max}, stations may influence the value of τ_c. Station control of τ_c by manipulation of p_{max} is obviously limited. For example, let us assume that p is fixed at 1 and that we have stations each generating packets at a rate $<1/\tau_c$. Increasing p will not change the cycle length since packets will be transmitted before a queue can form. On the other hand, increasing p for heavily loaded stations will lead to an increase of τ_c provided τ_c is less than the accepted maximum.") *See, e.g.*, p. 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.") *See, e.g.*, p. 1432 ("ACCESS-A station has a connection. Stations that already have access take the first free slot available to them after the appropriate START. Allocation of freed up slots on a reasonably equitable basis would proceed as follows. Stations would be aware of say n slots becoming free from the position of the END bit on the return line. Note, no END is issued if the class is full. Stations in the DEFER state would be permitted to compete for the n empty slots at the end of the subcycle. This will favor stations close to the head end. However, a large degree of fairness is achieved by permitting stations to switch from the WAIT to DEFER state only when two consecutive ENDS are encountered for that subcycle. This will only occur when all traffic currently in DEFER state has been granted access. At this point, traffic in the WAIT state would switch to DEFER and then vie for empty slots as they become available. This strategy is related to the snapshot algorithm. (iv) Continuation-In contrast to blocking, continuation requires that traffic not able to access the link in the previous cycle be served before any new traffic is accommodated. This may be achieved in the following manner. Assume that the class type is non-blocking. If the head station should issue a new START before all traffic of the class has been served, the end station will not detect the end of the cycle and hence will not issue END = 1. The absence of an END = 1 would indicate to the head station that the p registers of the stations in that class should not be reset on the next cycle (i.e., the stations would not switch from WAIT to DEFER). Thus, in the following cycle, remaining traffic would be served. For centralized

	control, the START for this traffic type could contain an additional bit to indicate whether the previous cycle is being continued for deferring tragic or a fresh cycle is being started for new traffic. For distributed control, each station could keep track of the sequence of STARTS and ENDS. It is important that the control strategy be adaptive to changing traffic conditions. We expect that the traffic mix will change relatively slowly-over a period of seconds rather than ms. Thus, it would be feasible to have the adaptation achieved by a server process. The control algorithm could be implemented as completely distributed, completely centralized, or somewhere in between. Economics and reliability will dictate, to a large extent, where the control should be placed. Nevertheless, a hybrid strategy would seem more in the spirit of the current design. For example, selection is probably best achieved by having the head station transmit the appropriate START code (centralized, but perhaps assumable), whereas traffic assignment and continuation is probably best achieved by having each station read and operate on the END field (distributed).")
4. An apparatus for assembling a dynamic time division multiplexing bit stream comprising,	Fasnet discloses an apparatus for assembling a dynamic time division multiplexing bit stream. *See, e.g.*, p. 1415 ("An integrated transmission system simplifies the implementation of services that utilize different types of traffic. Examples are voice annotated electronic mail and interactive use of voice and facsimile.")
generating means for generating a train of frames	Fasnet discloses an apparatus with a generating means for generating a train of frames. *See, e.g.*, p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.") *See, e.g.*, p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B.

<table>
<tr>
<td></td>
<td>The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.")</td>
</tr>
<tr>
<td>wherein each frame includes a transmission overhead field containing timing information and an empty payload field,</td>
<td>Fasnet discloses an apparatus wherein each frame includes a transmission overhead field containing timing information and an empty payload field.

See, e.g., p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium. The main objective in the design of this field is to control access among all active stations in an efficient, reliable, and fair manner. The frame start and frame end delimiters are unnecessary, since the stations are kept in tight bit and frame synchronization (see Section 5.1). The duration of the frame is referred to as a slot.")

See, e.g., Table 1:

Table I—Protocol and frame structures
<table>
<tr><th></th><th>Protocol Structure</th><th>Frame Structure</th></tr>
<tr><td>Data link layer</td><td>Logical link control sublayer
Media access control sublayer</td><td>DA/SA/LC/IU
FS/AC/DA/SA/LC/IU/FCS/FE</td></tr>
<tr><td>Physical layer</td><td>Physical layer signaling</td><td>FS/AC/DA/SA/LC/IU/FCS/FE</td></tr>
</table>
FS: Frame starting delimiter
AC: Access control field
DA: Destination address
SA: Source address
LC: Link control field
IU: Information unit from network layer
FCS: Frame check sequence
FE: Frame ending delimiter

See, e.g., Fig. 3:</td>
</tr>
</table>

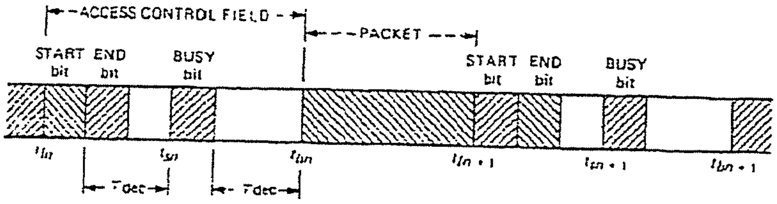


Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer.

See, e.g., p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.");

See, e.g., p. 1423-24 ("Typical operation of Fasnet for lines of 2.5-km individual length, 100 Mb/s bandwidth, and 200-bit frame length is shown in Fig. 5. It shows the time-space relation of the frames on each line. The horizontal axis represents time divided into slots A1, A2, A3, . . . for line A and B1, B2, B3, . . . for line B. The vertical axis represents the physical locations of the active stations S1, S2, S3, S4, and S5 with S1 and S5 serving, additionally, as end stations. The electrical line length is five frames. Station S1 initiates the cycle in frame A1, and access passes from S1 to S2 to S3 to S4. When the end station, S5, senses BUSY = 0 in frame A5, it sets END = 1 in frame B9. Receipt of this frame by S1 causes it to initiate a new cycle in A14. Similarly, a cycle on line B starts at B1. Assume that S5 and S4 are permitted access for up to two and three packets, respectively. Station S1 senses BUSY = 0 in frame B8 and sets END = 1 in A13. Receipt of this frame by S5 causes it to start a new cycle in B17.")

See, e.g., pp. 1425-26 ("V. IMPLEMENTATION CONSIDERATIONS

The design criteria previously stressed in the introduction affect the implementation in important ways. In particular, the requirement to operate at high speeds and the unidirectional operation of the bus affect the design of the synchronization system; in turn, the type of synchronization and the use of directional couplers impact the choice of the line code that is used.

5.1 Synchronization

	Bus systems in which signals travel in both directions on the line require the receiving stations to adapt to the signals transmitted by the sending station because the amplitude, dispersion, and phasing of the received signal vary depending upon the position of the transmitting station on the line. Synchronization can be achieved very quickly when the signaling rate is low relative to the bandwidth of the transmission medium. At higher signaling rates, synchronization needs to be more accurate to achieve good error performance. Ethernet specifies a synchronization preamble of 64 bits and for higher transmission rates an even longer sequence may be required. Thus, for short messages efficiency would be significantly reduced. Using a unidirectional bus, each station can be synchronized to a common clock issued from the head station. Thus, if all stations add signals to the cable in phase with the transmitting clock, stations will receive the signals in correct phase. Similarly, fixed gain and frequency compensation can be employed. The problem of reliability can be overcome by giving each station the ability to supply clock. The clock drive would be inhibited by detection of, and locking to, an incoming clock. Initial tests have shown that a simple, cost-effective method of synchronization is to synchronize to a continuously injected pilot tone placed at the high end of the signaling band. The synchronizing function then assumes a negligible fraction of the transmission capacity. In addition to bit synchronization, frame synchronization is also required. This is achieved by sending periodically a synchronizing bit pattern. Design is simplified if this is sent after an integral number of frames, say 64 or 128. With tight bit and frame synchronization, successive frames may be butted together without a gap.")
Processing means for processing data from a plurality of sources into packet format, and	Fasnet discloses an apparatus with a processing means for processing data from a plurality of sources into packet format. *See, e.g.*, p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the

<table>
<tr>
<td></td>
<td>
physical medium.")

See, e.g., Table 1:

<table>
<caption>Table I—Protocol and frame structures</caption>
<tr><th></th><th>Protocol Structure</th><th>Frame Structure</th></tr>
<tr><td>Data link layer</td><td>Logical link control sublayer
Media access control sublayer</td><td>DA/SA/LC/IU
FS/AC/DA/SA/LC/IU/FCS/FE</td></tr>
<tr><td>Physical layer</td><td>Physical layer signaling</td><td>FS/AC/DA/SA/LC/IU/FCS/FE</td></tr>
</table>

FS: Frame starting delimiter
AC: Access control field
DA: Destination address
SA: Source address
LC: Link control field
IU: Information unit from network layer
FCS: Frame check sequence
FE: Frame ending delimiter

See, e.g., Fig. 3:

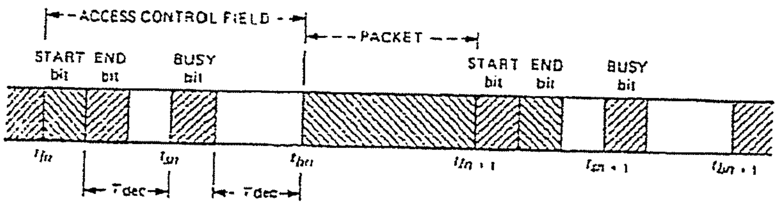


Fig. 3—The frame structure of Fasnet. Each frame consists of (*i*) an access control field containing START, END, and BUSY bits; and (*ii*) the packet as provided by the logical link sublayer.

See, e.g., p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.")

See, e.g., 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.")
</td>
</tr>
<tr>
<td>Inserting means for receiving said train of frames and for inserting each of said packets comprised of data from one of said plurality of sources</td>
<td>Fasnet discloses an apparatus with an inserting means for receiving a train of frames and for inserting each packet comprised of data from one of a plurality of sources into any empty payload field of any of the frames available to the inserting means to form a bit stream so that data from each of said sources can be transmitted at its own desired bit rate via the bit stream and so that data from the plurality of sources can be transmitted simultaneously via said bit stream.</td>
</tr>
</table>

into any empty payload field of any of said frames available to said inserting means to form said bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream.	*See, e.g.*, p. 1419 ("If a station has priority, it is given permission to access the line for an integral number of slots. In this manner, the active stations can access the line for a specified duration in the order in which they are physically located on the line.") *See, e.g.*, p. 1427 ("VI. IMPROVING UTILIZATION As can be seen from (I), efficiency increases (i) as cycle length increases and (ii) as the idle period at the end of each cycle (intercycle gap) decreases. At the expense of some increase in complexity, techniques may be devised to improve utilization by increasing cycle length or reducing intercycle gap. 6.1 Control of cycle length Since START = 1 may be read by all stations, the length of the last cycle, τc, may be determined by any station. As previously described, each station may transmit up to p_{max} packets per access. Thus, by controlling p_{max}, stations may influence the value of τ_c. Station control of τ_c by manipulation of p_{max} is obviously limited. For example, let us assume that p is fixed at 1 and that we have stations each generating packets at a rate $<1/\tau_c$. Increasing p will not change the cycle length since packets will be transmitted before a queue can form. On the other hand, increasing p for heavily loaded stations will lead to an increase of τ_c provided τ_c is less than the accepted maximum.") *See, e.g.*, p. 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream.") *See, e.g.*, p. 1432 ("ACCESS-A station has a connection. Stations that already have access take the first free slot available to them after the appropriate START. Allocation of freed up slots on a reasonably equitable basis would proceed as follows. Stations would be aware of say n slots becoming free from the position of the END bit on the return line. Note, no END is issued if the class is full. Stations in the DEFER state would be permitted to compete for the n empty slots at the end of the subcycle. This will favor stations close to the head end. However, a large degree of fairness is achieved by permitting stations to switch from the WAIT to DEFER state only when two consecutive ENDS are encountered

	for that subcycle. This will only occur when all traffic currently in DEFER state has been granted access. At this point, traffic in the WAIT state would switch to DEFER and then vie for empty slots as they become available. This strategy is related to the snapshot algorithm. (iv) Continuation-In contrast to blocking, continuation requires that traffic not able to access the link in the previous cycle be served before any new traffic is accommodated. This may be achieved in the following manner. Assume that the class type is non-blocking. If the head station should issue a new START before all traffic of the class has been served, the end station will not detect the end of the cycle and hence will not issue END = 1. The absence of an END = 1 would indicate to the head station that the p registers of the stations in that class should not be reset on the next cycle (i.e., the stations would not switch from WAIT to DEFER). Thus, in the following cycle, remaining traffic would be served. For centralized control, the START for this traffic type could contain an additional bit to indicate whether the previous cycle is being continued for deferring tragic or a fresh cycle is being started for new traffic. For distributed control, each station could keep track of the sequence of STARTS and ENDS. It is important that the control strategy be adaptive to changing traffic conditions. We expect that the traffic mix will change relatively slowly-over a period of seconds rather than ms. Thus, it would be feasible to have the adaptation achieved by a server process. The control algorithm could be implemented as completely distributed, completely centralized, or somewhere in between. Economics and reliability will dictate, to a large extent, where the control should be placed. Nevertheless, a hybrid strategy would seem more in the spirit of the current design. For example, selection is probably best achieved by having the head station transmit the appropriate START code (centralized, but perhaps assumable), whereas traffic assignment and continuation is probably best achieved by having each station read and operate on the END field (distributed).")

requisite intent to deceive may be inferred because one or more individuals substantively involved in the prosecution of the application for the '633 patent knew of the materiality of Annex 7.

Lucent further states that its investigation is ongoing and that it will supplement this response pursuant to FEDERAL RULE OF CIVIL PROCEDURE 26(e) as it discovers additional responsive information.

YOUNG CONAWAY STARGATT & TAYLOR, LLP

John W. Shaw (No. 3362)
jshaw@ycst.com
Montè T. Squire (No. 4764)
msquire@ycst.com
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, Delaware 19899-0391
(302) 571-6600

Attorneys for Lucent Technologies Inc.

Of Counsel:

Steven C. Cherny
Latham & Watkins LLP
885 Third Avenue, Suite 1000
New York, NY 10022
(212) 906-1200

David Nelson
Israel Sasha Mayergoyz
David C. McKone
Latham & Watkins LLP
Sears Tower, Suite 5800
Chicago, IL 60606
(312) 876-7700

Dated: March 23, 2006

CERTIFICATE OF SERVICE

I, Monté T. Squire, Esquire, hereby certify that on March 23, 2006, I caused to be served true and correct copies of the foregoing document on the party listed below:

BY HAND DELIVERY

Steven J. Balick, Esquire
Ashby & Geddes
222 Delaware Avenue, 17th Floor
Wilmington, DE 19801

BY FEDEX

Donald R. Dunner, Esquire
Finnegan, Henderson, Farabow,
Garrett, & Dunner, L.L.P.
901 New York Ave., N.W.
Washington, D.C. 20001

York M. Faulker, Esquire
Finnegan, Henderson, Farabow,
Garrett, & Dunner, L.L.P.
Two Freedom Square
11955 Freedom Drive
Reston, VA 20190

YOUNG CONAWAY STARGATT & TAYLOR, LLP

John W. Shaw (No. 3360)
Karen E. Keller (No. 4489)
Monté T. Squire (No. 4764)
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, Delaware 19899
(302) 571-6600
msquire@ycst.com